DESCRIPTION

PHASE-SELECTIVE TYPE FREQUENCY MODULATOR AND

5   PHASE-SELECTIVE TYPE FREQUENCY SYNTHESIZER

TECHNICAL FIELD

The present invention relates to a phase-selective type

frequency modulator and a phase-selective type frequency

10   synthesizer capable of reducing electromagnetic interference

(hereinafter, referred to as "EMI") in electronic equipment

which transmits image data, etc.

BACKGROUND ART

15   With the rapid operation of electronic equipment, the

EMI in the electronic equipment becomes a problem and the

reduction of the EMI is required. As one technology for

reducing the EMI in electronic equipment, a method employing

a spread spectrum clock signal has been proposed. More

20   specifically, jitter is intentionally generated so that a

peak of a spectrum may not be generated at a particular

frequency, or a frequency is varied gradually with a cycle,

that provides no influence on the operation of the circuit,

for example, a cycle in a range from several of kilo Hertz

25   to several hundreds of kilo Hertz.

Fig. 17 is a functional block diagram showing a

configuration of a clock signal generator disclosed in

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Japanese Patent Application Publication JP-A-2001-148690. As shown in Fig. 17, the above-mentioned clock signal generator has a clock generating unit 2001 for generating m-phase clock signals S1m having a desired frequency and phases shifted

5 by a constant interval between adjacent two clock signals, a selector unit 2003 for selecting one of the m-phase clock signals S1m, and a dithering control unit 2002 for determining the selection in the selector unit 2003. The m-phase clock signals S1m generated in the clock generating unit 2001 are

10 supplied to the selector unit 2003 and taken out via an output terminal 2005. To the selector unit 2003, a control signal SEL is supplied from the dithering control unit 2002. The selector unit 2003 sequentially selects one of the m-phase clock signals S1m in accordance with the control signal SEL

15 and thus obtained clock signal S2 can be taken out from an output terminal 2004. The dithering control unit 2002 for controlling the selector unit 2003 generates a selection signal SEL such that the spectrum of the clock signal S2 obtained at the output terminal 2004 may spread over as wide

20 as possible.

Fig. 18 is a circuit block diagram showing a specific configuration example of the dithering control unit 2002. As shown in Fig. 18, the dithering control unit 2002 includes eight D-type flip-flops 2031 to 2038 forming a serial ring,

25 and three OR circuits 2041 to 2043. When one signal of output signals S0 to S4 is at a high level, other four signals are made to be at low level, and the high-level moves among these

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signals per cycle of a clock signal CK.

Fig. 19 is a block diagram showing a specific configuration example of the selector unit 2003. The selector unit 2003 includes five switch circuits 2051 to 2055 and a buffer circuit 2056. In synchronization with the above-mentioned output signals S0 to S4, one of five-phase clock signals DC0 to DC4 at ΔT intervals is selected, and a modulated clock signal is generated and outputted via the buffer circuit 2056.

Fig. 20 shows an operation waveform example of the above-mentioned clock signal generator. As shown in Fig. 20, in a time period A, the clock signals are selected in the order of DC0, DC1, DC2, SC3, DC4 and the period of the modulated clock signal S2 becomes $T+\Delta T$. On the other hand, in a time period B, the clock signals are selected in the order of DC4, DC3, DC2, SC1, DC0 and the period of the modulated clock signal S2 becomes $T-\Delta T$. Here, "T" is defined as an inverse number of a frequency f_{CK} of a system clock signal, and, hereinafter, "T" is used in the same sense. Since the operations in the time periods A and B are repeated, $+\Delta T$ and $-\Delta T$ are cancelled so that the modulation period T_{mod} (not shown) becomes T_{mod} = 8 × T. According to the above-mentioned clock signal generator, a clock signal can be outputted in which peaks on the spectrum are spread, and the EMI can be reduced by operating the electrical equipment employing the clock signal.

However, in the case where the above-mentioned clock

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signal generator is used, there is a problem as described below. The problem will be explained by referring to Fig. 21. Fig. 21 shows the problem in the operation of the above-mentioned clock signal generator. As shown in Fig. 21,

5   when the edges of the m-phase clock signals S1m (a rising edge 2101 and a trailing edge 2103 are shown in Fig. 21) and the edges of the selection signal SEL overlap one another, the operations of the switch circuits 2051 to 2055 (switching between "0" and "1") provided in the selector unit 2003 as

10   shown in Fig. 19 becomes defective and the waveform of the modulated clock signal becomes deteriorated. That is, within 360 degrees as a clock phase corresponding to one period of the system clock signal as shown in Fig. 21 (the range shown by an arrow), a range of a clock phase of the system clock

15   signal that can be actually changed is restricted to a range obtained by subtracting a range in consideration of a predetermined interval from 180 degrees, i.e., less than 180 degrees.

    Here, referring to Figs. 22A to 22C, the relationship

20   between the modulation period and the spectrum intensity of the clock signal will be explained. Fig. 22A shows the relationship between the spectrum intensity and the frequency when the clock signal is not modulated. Fig. 22B shows the relationship between the spectrum intensity and the frequency

25   when the modulation period is short, that is, 1/Tmod is large. Fig. 22C shows the relationship between the spectrum intensity and the frequency when the modulation period is long, that

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is, 1/Tmod is small. Here, "Tmod" represents a modulation period and "T" is an inverse number of the frequency f_{CK} of the system clock signal.

As shown in Fig. 22A, when the clock signal is not modulated, a spectrum peak 2201 is observed in the position where $f = 1/T$. In the case where the clock signal is modulated so that the modulation clock frequency may become $T-\Delta T$ and $T+\Delta T$ for spreading the spectrum as shown in Fig. 22A, peaks are expected to appear at frequencies $f = 1/(T+\Delta T)$ and $f = 1/(T-\Delta T)$. However, almost all spectrum components at frequencies $f = 1/(T+\Delta T)$ and $f = 1/(T-\Delta T)$ are concentrated at the peak 2201 at a frequency $f = 1/T$ when the modulation period is short, i.e., $1/Tmod > \Delta f$, and the power dispersion never occurs as shown in Fig. 22B. Because, according to the nature of the Fourier transform, as to the waveform changing with a cycle of 1/Tmod, peaks appear at frequency intervals of 1/Tmod. On the other hand, when the modulation period is long as shown in Fig. 22C, i.e., $1/Tmod < \Delta f$, the spectrum components at frequencies $f = 1/(T+\Delta T)$ and $f = 1/(T-\Delta T)$ appear as peaks. That is, in addition to the peak 2201 at the frequency $f = 1/T$, a peak 2217 and a peak 2215 appear between the frequencies $f = 1/(T+\Delta T)$ and $f = 1/(T-\Delta T)$ at frequency intervals of 1/Tmod. With the power dispersion, the intensity of the peak 2201 at the frequency $f = 1/T$ becomes lower compared to the intensity of the peak 2201 as shown in Figs. 22A and 22B, and the occurrence of power dispersion is seen.

Considering a condition under which the modulation

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effect is seen, it is necessary that the frequency interval at which the peaks appear is shorter than the frequency interval between $1/T$ and $1/(T\pm\Delta T)$. That is, the following expression (1) is required to hold.

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$$1/Tmod < ABS(1/T - 1/(T\pm\Delta T)) \approx \Delta T/T^2 \quad ... \quad (1)$$

Where ABS(X) represents an absolute value of X.

Here, given that the number of phases of multiphase clock signals is N, the modulation period Tmod is expressed by the following expression (2).

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$$Tmod = 2N \times T \quad ... \quad (2)$$

With the expressions (1) and (2), the following expression (3) can be introduced.

$$T/2 < N \times \Delta T \quad ... \quad (3)$$

Here, $N \times \Delta T$ corresponds to the range in which the phase

15 is valuable in the circuits as shown in Fig. 17-19, and a phase valuable range of at least 180 degrees is required as described above.

DISCLOSURE OF THE INVENTION

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Accordingly, in view of the above-mentioned points, an object of the present invention is to provide a phase-selective type frequency modulator and a phase-selective type frequency synthesizer capable of easing the restriction on a phase range of a modulated clock signal.

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In order to solve the above-mentioned problems, a phase-selective type frequency modulator according to one aspect of the present invention includes: multiphase clock

signal generating means for generating N-phase clock signals having phase differences from each others; control means for sequentially activating one of first group of clock selection signals indicating a clock signal to be selected from the

5   N-phase clock signals outputted from the multiphase clock signal generating means, the first group of clock selection signals corresponding to the N-phase clock signals; edge appearance time adjusting means for adjusting a rising edge appearance time and/or a trailing edge appearance time of

10   the first group of clock selection signals outputted from the control means to output second group of clock selection signals corresponding to the N-phase clock signals outputted from the multiphase clock signal generating means; and modulated clock signal generating means for selecting one

15   clock signal from the N-phase clock signals in accordance with an activated state of the second group of clock selection signals outputted from the edge appearance time adjusting means to output the selected clock signal as a modulated clock signal.

20   Further, a phase-selective type frequency synthesizer according to one aspect of the present invention includes: control means for sequentially activating one of first group of clock selection signals indicating a clock signal to be selected from N-phase clock signals having phase differences

25   from each others, the first group of clock selection signals corresponding to the N-phase clock signals; edge appearance time adjusting means for adjusting a rising edge appearance

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time and/or a trailing edge appearance time of the first group

of clock selection signals outputted from the control means

to output second group of clock selection signals

corresponding to the N-phase clock signals; modulated clock

5   signal generating means for selecting one clock signal from

the N-phase clock signals in accordance with an activated

state of the second group of clock selection signals outputted

from the edge appearance time adjusting means to output the

selected clock signal; phase comparing means for comparing

10   a phase of a reference clock signal and a phase of the clock

signal selected by the modulated clock signal generating

means; and multiphase clock signal generating means for

generating the N-phase clock signals based on a comparison

result in the phase comparing means and outputting one of

15   the N-phase clock signals as a modulated clock signal.

        According to the present invention, since the

restriction on the phase range of the modulated clock signal

can be eased, the EMI can be further reduced.

20   BRIEF DESCRIPTION OF THE DRAWINGS

        Advantages and features of the present invention will

be clear by considering the following detailed description

and the drawings in relation. In these drawings, the same

reference numerals indicate the same component elements.

25   Fig. 1 is a block diagram showing a configuration of

a phase-selective type frequency modulator according to a

first embodiment of the present invention;

Fig. 2 is a block diagram showing a configuration of a phase-selective type frequency synthesizer according to the first embodiment of the present invention;

Fig. 3 is a block diagram showing a configuration example of a multiphase clock signal generating circuit as shown in Fig. 1;

Fig. 4 is a block diagram showing a configuration example of a multiphase VCO as shown in Fig. 2;

Fig. 5 shows a configuration example including a modulated clock signal generating circuit and an edge appearance time adjustment circuit as shown in Fig.1;

Fig. 6 shows a configuration example including a modulated clock signal generating circuit and an edge appearance time adjustment circuit as shown in Fig. 2;

Figs. 7A and 7B show configuration examples of a switch circuit in Fig. 5;

Fig. 8 shows a modified example of the modulated clock signal generating circuit and the edge appearance time adjustment circuit as shown in Fig. 5 or 6;

Fig. 9 is a timing chart for explaining an operation of the modulated clock signal generating circuit and the edge appearance time adjustment circuit;

Fig. 10 is a timing chart for explaining an operation of the modulated clock signal generating circuit and the edge appearance time adjustment circuit;

Fig. 11 is a block diagram showing a configuration example of a control circuit as shown in Fig. 1 or 2;

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Fig. 12 shows an up/down ring register as shown in Fig. 11;

Fig. 13 is a block diagram showing another configuration example of the control circuit as shown in Fig. 1 or 2;

5   Fig. 14 is a timing chart showing an operation of the control circuit as shown in Fig. 13;

Fig. 15 is a block diagram showing a configuration of a three-valued $\Delta\Sigma$ modulator as shown in Fig. 11;

Fig. 16 is a block diagram showing a configuration of 10   a phase-selective type frequency modulator according to a second embodiment of the present invention;

Fig. 17 is a block diagram showing a configuration of a conventional clock signal generator;

Fig. 18 is a block diagram showing a configuration example 15   of a dithering control unit in Fig. 17;

Fig. 19 is a block diagram showing a configuration of a selector unit in Fig. 17;

Fig. 20 is an operation waveform chart of the clock signal generator in Fig. 17;

20   Fig. 21 is a diagram for explaining a problem of the clock signal generator in Fig. 17 in view of the operation waveform; and

Fig. 22 is a diagram for explaining a problem of the clock signal generator in Fig. 17 in view of spectrum spread.

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BEST MODE FOR CARRYING OUT THE INVENTION

In a phase-selective type frequency modulator and a

phase-selective type frequency synthesizer according to the present invention, in order to generate a modulated clock signal in which the restriction of phase valuable range is eased to reduce the EMI, a circuit is formed such that a rising

5   edge appearance time and/or a trailing edge appearance time of one clock signal selected from N-phase clock signals and a rising edge appearance time and/or a trailing edge appearance time of a clock selection signal for selecting the clock signal may have time lag and may not overlap one another.

10   Here, in the case where a number "N" of phases of the N-phase clock signals is an integer number equal to or more than four, the phase-selective type frequency modulator and the phase-selective type frequency synthesizer according to the present invention exert effects.

15   More specifically, when a modulated clock signal is generated by selecting one clock signal (referred to as a "first clock signal") from the N-phase clock signals from 1 to N having different phases, as a clock selection signal for selecting the first clock signal, a second clock selection

20   signal is generated which has the edge appearance time adjusted based on another clock signal (referred to as a "second clock signal") having a different phase from the first clock signal among the N-phase clock signals and which the first clock signal indicates to be selected. According to the activated

25   state of the second clock selection signal (e.g., high-level or low-level), one of the N-phase clock signals CK1 to CKN is selected and the selected clock signal is outputted as

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a modulated clock signal.

Thereby, the rising edge appearance time and/or the trailing edge appearance time of the first clock signal and the rising edge appearance time and/or the trailing edge appearance time of the second group of clock selection signals for selecting the first clock signal can be arbitrarily shifted.

Based on the above consideration, a phase-selective type frequency modulator according to embodiments of the present invention will be explained by referring to the drawings as below.

Fig. 1 shows a configuration of a phase-selective type frequency modulator according to a first embodiment of the present invention. As shown in Fig. 1, a phase-selective type frequency modulator 100 according to the first embodiment of the present invention includes a multiphase clock signal generating circuit 101 for generating multiphase clock signals, a modulated clock signal generating circuit 102 for performing modulation operation by selecting one clock signal from the multiphase clock signals, an edge appearance time adjustment circuit 103, and a control circuit 104 having a clock selection signal generating circuit 105 and a control logic circuit 106 for controlling it. A number "N of phases of the multiphase clock signals is, for example, 6, 12, or the like. The modulated clock signal generating circuit 102

outputs a selected clock signal SELCLK as a modulated clock signal MCK.

Fig. 2 shows a configuration of a phase-selective type frequency synthesizer employing the phase-selective type frequency modulator in Fig. 1. A phase-selective type frequency synthesizer 110 modulates an inputted reference clock signal (REFCLK) 111 to output it as a modulated clock signal 120. The phase-selective type frequency synthesizer includes a phase comparison circuit 115 having a phase detector (PD) 112, a charge pump 113, and a loop filter 114 such as a low pass filter (LPF), and a multiphase (N-phase) voltage controlled oscillator (VCO) 116. Furthermore, the phase-selective type frequency synthesizer includes a modulated clock signal generating circuit 102, an edge appearance time adjustment circuit 103, and a control circuit 104 having a clock selection signal generating circuit 105 and a control logic circuit 106 similar to those shown in Fig. 1. The output of the modulated clock signal generating circuit 102 is controlled by the phase comparison circuit 115 which compares a phase of a clock signal fed back via a divider 117 and a phase of the reference clock signal (REFCLK) 111. A clock signal CK1 as one of the output of the multiphase VCO 116 is divided in a divider 118, and the modulated clock signal 120 is outputted which has a frequency modulated into a desired value.

The modulated clock signal generating circuit 102 selects one of N-phase clock signals outputted from the

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multiphase VCO 116 to output it as a selected clock signal SELCLK. By comparing a phase of the feed back signal and a phase of the reference clock signal (REFCLK) 111 in the phase comparison circuit 115 and controlling the output of the

5   modulated clock signal generating circuit 102, the modulated clock signal 120, which has a frequency modulated into a desired value, is generated based on the clock signal CK1 as one of outputs of the multiphase VCO 116.

In the above-mentioned configuration, when the selection

10 in the selector of the modulated clock signal generating circuit 102 is not changed, the frequency of the modulated clock signal is expressed by the following expression.

$$f0 = f_{REFCLK} \cdot M/N$$

When the selection in the selector is shifted, for example,

15 backwardly one at a time, the frequency of the modulated clock signal is controlled to be $f_{max} = f0 \cdot 13/12$. Oppositely, when the selection in the selector is forwardly shifted, for example, forwardly one at a time, the frequency of the modulated clock signal is controlled to be $f_{min} = f0 \cdot 11/12$. By mixing the

20 manners of shifting selection in the selector, the frequency of the modulated clock signal can be controlled to be an arbitrary value between f_{min} and f_{max}.

By controlling the manners of shifting selection in the selector by using delta sigma modulation according to

25 frequency data, it is possible to cause the frequency of the modulated clock signal to be a value set by the frequency data. The order of the delta sigma modulation may be first

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order, second order or higher order. However, the accuracy in the case of second order is higher than that in the case of first order, and in the case of third or higher order, the circuit is scaled up although the effect is not so different

5   from that in the case of second order. Therefore, about second order is desirable.

Fig. 3 shows a configuration example of the multiphase clock signal generating circuit 101 as shown in Fig. 1. The multiphase clock signal generating circuit 101 as shown in

10   Fig. 3 has three differential amplifiers 201 to 203 and six comparators 211 to 216. The three differential amplifiers 201 to 203 form a ring oscillator. The six comparators 211 to 216 compare non-inversion outputs and inversion outputs of the differential amplifiers 201 to 203, which have delays,

15   in the comparators 211 to 216 to convert them into six-phase clock signals CK1 to CK6. By setting all delay times of the differential amplifiers 201 to 203 to be equal, the six-phase clock signals CK1 to CK6 can be made at equal phase intervals.

Fig. 4 shows a configuration example of the multiphase

20   VCO 116 as shown in Fig. 2. The multiphase VCO 116 as shown in Fig. 4 has a ring oscillator formed by six differential amplifiers 221 to 226 and twelve comparators 231 to 242. By the control voltages of the differential amplifiers 221 to 226, delay times at the respective differential amplifiers

25   can be changed and the frequency can be controlled. Further, by performing level conversion on the outputs of each differential amplifier by using two comparators for normal

and inversion, twelve-phase clock signals CLK1 to CLK12 are generated.

Fig. 5 shows a configuration example including the modulated clock signal generating circuit 102 and the edge appearance time adjustment circuit 103 as shown in Fig.1. As shown in Fig. 5, the edge appearance time adjustment circuit 103 includes flip-flop circuits 801 to 806 and the modulated clock signal generating circuit 102 includes switch circuits 811 to 816 corresponding to the flip-flop circuits 801 to 806 and a buffer circuit 821 commonly provided for outputs thereof.

To the respective input terminals of the flip-flop circuits 801 to 806, corresponding first group of clock selection signals SEL1 to SEL6 are inputted, and, to the clock signal terminals thereof, there are inputted respective clock signals CK1 to CK6 having a phase difference within a predetermined range from the clock signals selected in accordance with the first group of clock selection signals SEL1 to SEL6. For example, the clock selection signal SEL1 is inputted to the input terminal of the flip-flop circuit 801 and the clock signal CK5 is inputted to the clock signal terminal thereof. Similarly, the clock selection signal SEL2 is inputted to the input terminal of the flip-flop circuit 802 and the clock signal CK6 is inputted to the clock signal terminal thereof.

Thereby, the first group of clock selection signals SEL1 to SEL6 inputted to the flip-flop circuits 801 to 806,

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respectively, are latched in synchronization with respective clock signals having a phase leading by T/3 (120 degrees) the clock signals CK1 to CK6 respectively selected by the first group of clock selection signals SEL1 to SEL6, and the

5   latched signals are outputted as second group of clock selection signals (switch control signals) SSEL1 to SSEL6 for controlling ON/OFF of the corresponding first to sixth switch circuits 811 to 816.

To prevent edge appearance times from overlapping

10 between the second group of clock selection signals SSEL1 to SSEL6 and respective clock signals selected thereby, the widest margin is obtained in the case where the phase difference between the selected clock signal and the clock signal to be used for latching the first group of clock selection signals

15 in the flip-flop circuits is set on about 90 degrees. Fig. 5 shows the case where the phase difference is 120 degrees as an example.

To the input sides of the switch circuits 811 to 816, corresponding clock signals CK1 to CK6 are inputted, ON/OFF

20 control is performed according to the second group of clock selection signals SSEL1 to SSEL6, and the selected one clock signal is transmitted to the output side. The output sides of the switch circuits 811 to 816 are commonly connected and the selected clock signal is outputted as a selected clock

25 signal SELCLK via a buffer circuit 821.

Fig. 6 shows a configuration example including a twelve-phase modulated clock signal generating circuit 102

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and the edge appearance time adjustment circuit 103. Since the edge appearance time adjustment circuit 103 adjusts the activation timing of second group of clock selection signals SSEL1 to SSEL12, the edge appearance times are constantly

5   at fixed intervals between the second group of clock selection signals and the selected respective clock signals, and the edges of both never overlap.

In the edge appearance time adjustment circuit 103, the first group of clock selection signals SEL1 to SEL12 are latched

10   in synchronization with respective clock signals having a predetermined phase difference from the corresponding clock signals CK1 to CK12, and outputted as second group of clock selection signals SSEL1 to SSEL12 in which edges have been adjusted. The modulated clock signal generating circuit 102

15   selects one of the clock signals CK1 to CK12 according to the second group of clock selection signals SSEL1 to SSEL12 and outputs it as a selected clock signal SELCLK.

Figs. 7A and 7B show configuration examples of the switch circuit 811 within the modulated clock signal generating

20   circuit 102 in Fig. 5. The switch circuit as shown in Fig. 7A is an analog switch of CMOS circuits and has an N-channel MOS transistor 903, a P-channel MOS transistor 902 and an inverter 901. To the control terminal (gate terminal) of the N-channel MOS transistor 903, one of the second group of clock

25   selection signals (switch control signals), e.g., a clock selection signal SSEL1 as shown in Fig. 5 is inputted. To the gate terminal of the P-channel MOS transistor 902, the

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clock selection signal SSEL1 inversed by the inverter 901 is inputted. When the clock selection signal SSEL1 is set at a high level, the analog switch becomes conductive and the clock signal CK1 inputted to the analog switch is

5   transmitted to the output terminal OUT of the analog switch.

The switch circuit as shown in Fig. 7B employs an N-channel MOS transistor 904, and a clock selection signal SSEL1 is inputted to the gate terminal of the N-channel MOS transistor 904. When the second clock selection signal SSEL1 is at a

10   high level, the clock signal CK1 inputted to the switch circuit is transmitted to the output terminal OUT of the switch circuit.

By the way, the switch circuits 812 to 816 and the switch circuits in Fig. 6 may be formed similarly to that shown in Fig. 7A or 7B.

15   Fig. 8 shows a modified example of the modulated clock signal generating circuit and the edge appearance time adjustment circuit as shown in Fig. 5 or 6. In Fig. 8, differences from the configuration as shown in Fig. 5 or 6 are in the point where, to the clock signal input terminal

20   of a flip-flop circuit corresponding to the switch circuit 1011, a clock signal CK1 same as a clock signal inputted to the corresponding switch circuit 1011 is inputted, and the point where there is provided a delay circuit 1002 for delaying the clock signal CK1 inputted to the switch circuit 1011.

25   Practically, N circuits as above-mentioned are provided.

In the case of employing the configuration as shown in Fig. 8, a clock signal delayed by the delay circuit 1002 relative

to the clock signal CK1 is similarly inputted to the switch circuit 1011, and therefore, a clock signal different in edge appearance time from the clock signal CK1 inputted to the flip-flop circuit 1001 can be inputted to the switch circuit

5   1011.

Referring to Figs. 9 and 10, the operations of the above-mentioned modulated clock signal generating circuit and edge appearance time adjustment circuit will be described. In Figs. 9 and 10, waveforms of the first group of clock

10   selection signals SEL1 to SEL6, the second group of clock selection signals SSEL1 to SSEL6 as substantial selection signals for selecting one of the clock signals CK1 to CK6 in Fig. 5, for example, the clock signals CK1 to CK6 and the selected clock signal SELCLK are shown.

15   In Fig. 9, the clock signals CK1 to CK6 are shifted in the phase lagging direction. According to the second group of clock selection signals SSEL1 to SSEL6, one of the clock signals CK1 to CK6 is sequentially selected. The period of thus generated selected clock signal SELCLK becomes $T+\Delta T$.

20   The first group of clock selection signals SEL1 to SEL6 are signals in synchronization with the selected clock signal SELCLK. Accordingly, the second group of clock selection signals SSEL1 to SSEL6 are generated by latching the first group of clock selection signals SEL1 to SEL6 in

25   synchronization with other predetermined clock signals, respectively. In the example as shown in Fig. 9, with respect to the clock signal CK1, by latching the first clock selection

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signal SEL1 in synchronization with the rising edge of the clock signal CK5, the second clock selection signal SSEL1 is changed into at low level or high level. Further, with respect to the clock signal CK2, by latching the first selection

5   signal SEL2 in synchronization with the rising edge of the clock signal CK6, the second clock selection signal SSEL2 is changed into at low level or high level. Similarly, others of the second group of clock selection signals SSEL3 to SSEL6 are generated.

10   Here, as clearly seen in Fig. 9, edge appearance positions of the clock signal CK1 and the second clock selection signal SSEL1 generated in synchronization with the clock signal CK5 having a different phase from the clock signal CK1 (leading in phase by T/3, i.e., 120 degrees) are constantly at fixed

15   intervals and the edge appearance times never overlap. Accordingly, with respect to the selected clock signal SELCLK sequentially generated by one of the clock signals CK1 to CK6, the waveform of the selected clock signal never becomes deteriorated because the edge appearance times of the second

20   group of clock selection signals SSEL1 to SSEL6 and the edge appearance times of the respectively selected clock signals CK1 to CK6 never overlap even if the period T+ΔT continues so long. Thus, there is an advantage that selected clock signals SELCLK corresponding to CK1 → CK2 → CK3 → CK4 →

25   CK5 → CK6 → CK1 → ... can be continuously generated. In Fig. 9, there is a period in which all of the second group of clock selection signals SSEL1 to SSEL6 are at low level,

however, within the period, the outputs of the switch circuits are held by parasitic capacitances of elements and wirings.

In Fig. 10, as well as in Fig. 9, one clock signal is sequentially selected from the clock signals CK1 to CK6. However, the case is different in the point where the period of the generated selected clock signal SELCLK is T−ΔT. That is, the clock signals CK1 to CK6 are shifted in the phase leading direction. For example, as clearly seen in Fig. 10, edge appearance times of the clock signal CK1 and the clock selection signal SSEL1 generated based on the clock signal CK5 having a different phase from the clock signal CK1 (leading in phase by T/3, i.e., 120 degrees) are constantly at fixed intervals and the edge appearance times never overlap.

Accordingly, with respect to the selected clock signal SELCLK sequentially generated based on the clock signals CK1 to CK6, no problem arises however long the period T−ΔT continues. Thus, there is an advantage that selected clock signals SELCLK respectively corresponding to CK1 → CK2 → CK3 → CK4 → CK5 → CK6 → CK1 → ... can be continuously generated. Although the six-phase case has been described in the above description, they operate similarly in the twelve-phase case.

Fig. 11 shows a configuration example of a control circuit 104 for supplying the clock selection signals to the edge appearance time adjustment circuit 103. As shown in Fig. 11, the control circuit 104 includes a control logic circuit 106 having a frequency data generator 601 and a three-valued ΔΣ modulator 602, and a clock selection signal generating circuit

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105 having an up/down ring register 603. The ring register 603 causes the state transition in synchronization with the selected clock signal SECLK to generate the first group of clock selection signals SEL1 to SEL12. The frequency data

5 FData outputted from the frequency data generator 601 is inputted to the three-valued $\Delta\Sigma$ modulator 602 and converted into a three-valued control signal CSG. The up/down ring register 603 causes the selection transition forward or backward, or maintains it according to the control signal

10 CSG. Note that, in the phase-selective type frequency modulator as shown in Fig. 1, a period data generator is used in place of the frequency data generator.

Fig. 12 shows the up/down ring register 603 as shown in Fig. 11. The up/down ring register 603 has D-type flip-flop

15 circuits (D-FF) 501 to 512 and selector circuits 521 to 532 corresponding to these flip-flop circuits 501 to 512. The output terminals of the flip-flop circuits 501 to 512 are connected to the input terminals of the first group of clock selection signals SEL1 to SEL12 in the edge appearance time

20 adjustment circuit 103 (see Fig. 6), respectively.

The selector circuits 521 to 532 are formed of three-input one-output selector circuits and controlled by the control signal (selector signal) CSG as an output of the control logic circuit 106 (see Fig. 11). More specifically, the selector

25 circuits 521 to 532 are circuits for outputting one of three inputs in accordance with the three conditions of the control signal CSG. On the other hand, the flip-flop circuits 501

to 512 latch the outputs of the selector circuits 521 to 532 in synchronization with the selected clock signal SECLK outputted from the modulated clock signal generating circuit and output them as the first group of clock selection signals SEL1 to SEL12. Thereby, a signal at high level transitions among the first group of clock selection signals SEL1 to SEL12.

Fig. 13 shows another configuration example of the control circuit 104. The control circuit 104 includes a clock selection signal generating circuit 105 having an up/down counter 401 and a decoder 402, and a control logic circuit 106 for controlling the clock selection signal generating circuit 105. The clock selection signal generating circuit 105 outputs the first group of clock selection signals SEL1 to SEL12 in accordance with the value of the control signal supplied from the control logic circuit 106. Simultaneously, the clock selection signal generating circuit 105 shifts the clock selection signal to be activated to the forward one or backward one, or maintains without change in accordance with the value of the control signal supplied from the control logic circuit 106.

The control logic circuit 106 outputs a control signal CSG for controlling the up/down counter 401. The up/down counter 401 is a counter capable of incrementing or decrementing the value of the counter one at a time when receiving pulse. The up/down counter 401 operates in synchronization with the modulated clock signal (pulse signal) SELCLK, and changes the counter value CTV of the output

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at each time when receiving the control signal CSG such that

$1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow \ldots \rightarrow 11 \rightarrow 12 \rightarrow 1 \rightarrow 2 \rightarrow \ldots$ (UP), or

$12 \rightarrow 11 \rightarrow \ldots \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 12 \rightarrow 11 \rightarrow \ldots$ (DOWN).

The up/down counter 401 outputs a value corresponding

to one of the three operations of "UP", "DOWN" and "HOLD"

as a counter value CTV to the decoder 402. The decoder 402

activates one of the first group of clock selection signals

SEL1 to SEL12 at a high level among the first group of clock

selection signals SEL1 to SEL12 in correspondence with the

counter value CTV.

Fig. 14 shows the operation of the control circuit 104

as shown in Fig. 13. The operation of the control circuit

104 differs between the case where the value of the control

signal CSG represents "UP" and the case where the value of

the control signal CSG represents "DOWN". In the case where

the value of the control signal CSG represents "UP", the signal

at a high level among the first group of clock selection signals

SEL1 to SEL12 changes such that SEL1 $\rightarrow$ SEL2 $\rightarrow$ SEL3 $\rightarrow$ ...

as shown by an arrow AR1. On the other hand, in the case where

the value of the control signal CSG represents "DOWN", the

signal at high-level among the first group of clock selection

signals SEL1 to SEL12 changes such that SEL4 $\rightarrow$ SEL3 $\rightarrow$ SEL2

$\rightarrow$ ... as shown by an arrow AR2.

Fig. 15 shows the configuration of the three-valued $\Delta\Sigma$

modulator 602 as shown in Fig. 11. As shown in Fig. 15, this

$\Delta\Sigma$ modulation circuit has a quadratic configuration, and has

a first to fourth adders 701, 702, 704 and 705, delay circuits

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703 and 706 and a three-valued quantizer 707. The three-valued
quantizer 707 outputs one of the three values of $+\Delta$, 0, $-\Delta$
as the control signal CS in response to the input. With respect
to the selection of clock signal, when three values are

5   associated with "backward transition", "maintenance" and
"forward transition", the frequencies of the modulated clock
signals are controlled to be $f = f0 \cdot 13/12$, $f = f0$ and $f = f0 \cdot 11/12$,
respectively.

According to the configuration as shown in Fig. 15, by

10   inputting the value expressed by the following expression
as the frequency data FData, the frequency of the modulated
clock signal MCK can be controlled to be an arbitrary frequency
f1.

Frequency data = $\Delta \times (f1-f0)/(f0/12)$ ... (5)

15   Note that, in place of the three-valued $\Delta\Sigma$ modulator
as shown in Fig. 15, a one-bit $\Delta\Sigma$ modulator may be used. In
this case, one bit is associated with two of "backward
transition", "maintenance" and "forward transition".

Thus, frequency modulation can be realized by a simple

20   configuration. Further, generally, when the pulse width of
the change pump is large, the jitter of the PLL output tends
to be larger. On the other hand, in the modulated clock signal
generating circuit according to the embodiment, the phase
of the clock signal for the feed back can be finely controlled

25   by using the selector, and therefore, there is an advantage
that the jitter is reduced.

According to the above-mentioned modulated clock signal

generator according to the first embodiment of the present
invention, modulated clock signals with no restriction on
the phase valuable range can be generated and the EMI of
electronic equipment can be reduced.

5   Next, a phase-selective type frequency modulator
according to a second embodiment of the present invention
will be described by referring to Fig. 16. As shown in Fig.
16, the phase-selective type frequency modulator according
to the second embodiment has a multiphase clock signal
10 generating circuit 101, a modulated clock signal generating
circuit 102, an edge appearance time adjustment circuit 103
and a control circuit 104 as well as the phase-selective type
frequency modulator according to the first embodiment as shown
in Fig. 1. It differs from the circuit as shown in Fig. 1
15 in the point where a PLL 1205 is additionally connected to
the output of the modulated clock signal generating circuit
102. In the embodiment, a modulated clock signal MCK is
outputted from the PLL 1205. According to the embodiment,
the discrete cyclic change in the selected clock signal SELCLK
20 outputted from the modulated clock signal generating circuit
102 is filtered by a loop filter of the PLL 1205, and therefore,
a modulated clock signal in which frequency change is mild
can be obtained.

25 INDUSTRIAL APPLICABILITY
       The present invention can be utilized in a
phase-selective type frequency modulator and a

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phase-selective type frequency synthesizer to be used in electronic equipment for performing transmission of image data and so on.